CLAIMS:

1. In an Electronic device including Asynchronous Transfer Mode (ATM) switching capabilities or including interior fixed length packet/cell processing for use in telecommunication networks, a method for buffering incoming cells of packets, the cells are assigned, each, within Virtual Path Identifier (VPI) and Virtual Channel Identifier (VCI), such that all cells of the same packet bear the same VCI; the method comprising:

   (a) associating each VCI with data that include data item serving for packet efficiency mechanism;

   (b) storing in a data structure selected number from said data items;

   (c) for each incoming cell whose VCI is associated with data item that is stored in said data structure, constructing a search key that enables to access said data item at substantially O(1).

2. The method according to Claim 1, wherein said data item indicates an EPD/PPD state machine.

3. The method according to Claim 2, wherein said data item is 2-bit-long representing a packet efficiency mechanism realized as an EPD/PPD state machine.

4. The method according to Claim 3, wherein said data structure being an N over M memory table.

5. The method according to Claim 1, wherein said data structure being an N over M memory table.

6. The method according to Claim 5, wherein the number of VPs accommodated in said memory being P and the number of VCs accommodated within said memory being L such that the following algorithmic expression applies: $N*M/S = P*L$, where S being the size of the data item.

7. The method according to Claim 4, wherein the number of VPs accommodated in said memory being P and the number of VCs accommodated within said memory being L such that the following algorithmic expression applies: $N*M/2 = P*L$.

8. The method according to Claim 6, wherein said memory is configurable according to any P and L that meet said algorithmic expression.

9. The method according to Claim 7, wherein said memory is configurable according to any P and L that meet said algorithmic expression.

10. The method according to Claim 1, wherein said step (c) further including:

i) for each incoming cell assigning an interim code ECI, being a member of consecutive series, that is being indicative of the VPI;

ii) constructing a search key that includes said interim code ECI and VCI.

11. The method according to Claim 10, wherein said search key is constructed by concatenating said ECI and VCI.

12. The method according to Claim 10, wherein said ECI partially overwrites the VPI, and wherein there is provided the additional step of:

(d) restoring the VPI according to a translation table before the cell is delivered as an output from the buffer.

13. The method according to Claim 1, further comprising a step of:

testing a triggering condition which determines whether or not to apply said step (c).

14. The method according to Claim 1, wherein only data items with associated VCI value that exceeds 31 are stored in said data structure.

15. An Electronic device including Asynchronous Transfer Mode (ATM) switching capabilities or including interior fixed length packet/cell processing for use in telecommunication networks, the electronic device includes a buffer of incoming cells of packets, the cells are assigned, each, within Virtual Path Identifier (VPI) and Virtual Channel Identifier (VCI), such that all cells of the same packet bear the same VCI; the device comprising:

(a) each VCI is associated with data that include data item serving for packet efficiency mechanism

(b) storage medium storing data representative of data structure for storing selected number from said data items;

(c) processor associated with said storage medium configured to perform the processing that include: for each incoming cell whose VCI is associated with data item that is stored in said data structure constructing a search key that enables to access said data item at substantially O(1).

16. The system according to Claim 15, wherein said data item indicates an EPD/PPD state machine.

17. The system according to Claim 16, wherein said data item is 2-bit-long representing a packet efficiency mechanism realized as an EPD/PPD state machine.

18. The system according to Claim 17, wherein said data structure being an N over M table.

19. The system according to Claim 15, wherein said data structure being an N over M table.

20. The system according to Claim 19, wherein the number of VPs accommodated in said table being P and the number of VCs accommodated within said memory being L such that the following algorithmic expression applies: N*M/S = P *L, where S being the size of the data item.

21. The system according to Claim 18, wherein the number of VPs accommodated in said table being P and the number of VCs accommodated within said memory being L such that the following algorithmic expression applies: N*M/2 = P *L.

22. The system according to Claim 20, wherein said table is configurable according to any P and L that meet said algorithmic expression.

23. The system according to Claim 21, wherein said table is configurable according to any P and L that meet said algorithmic expression.

24. The system according to Claim 15, wherein said processor is further configured to perform the processing:

i) for each incoming cell assigning an interim code ECI, being a member of consecutive series, that is being indicative of the VPI;

ii) constructing a search key that includes said interim code ECI and VCI.

25. The system according to Claim 24, wherein said search key is constructed by concatenating said ECI and VCI.

26. The system according to Claim 24, wherein said ECI partially overwrites the VPI, and wherein the processor is further configured to:

restoring the VPI according to a translation table before the cell is delivered as an output from the buffer.

27. The system according to Claim 15, wherein said processor is further configured to:

testing a triggering condition which determines whether or not to apply said step (c).

28. The system according to Claim 15, wherein only data items with associated VCI value that exceeds 31 is stored in said data structure.

29. In an Electronic device including Asynchronous Transfer Mode (ATM) switching capabilities or including interior fixed length packet/cell processing for use in telecommunication networks, a program storage device readable by machine, tangibly embodying a program of instructions executable by the machine to perform method steps for buffering incoming cells of packets, the cells are assigned, each, within Virtual Path Identifier (VPI) and Virtual Channel Identifier (VCI), such that all cells of the same packet bear the same VCI; the method comprising:

(a) associating each VCI with data that include data item serving for packet efficiency mechanism

(b) storing in a data structure selected number from said data items;

(c) for each incoming cell whose VCI is associated with data item that is stored in said data structure, constructing a search key that enables to access said data item at substantially O(1).

30. In an Electronic device including Asynchronous Transfer Mode (ATM) switching capabilities or including interior fixed length packet/cell processing for use in telecommunication networks, a computer program product comprising a computer useable medium having computer readable program code embodied therein for buffering incoming cells of packets, the cells are assigned, each, within Virtual Path Identifier (VPI) and Virtual Channel Identifier (VCI), such that all cells of the same packet bear the same VCI; the computer program product comprising:

computer readable program code for causing the computer to associate each VCI with data that include data item serving for packet efficiency mechanism;

computer readable program code for causing the computer to store in a data structure selected number from said data items;

computer readable program code for causing the computer to for each incoming cell whose VCI is associated with data item that is stored in said data structure, constructing a search key that enables to access said data item at substantially O(1).